

**IN THE CLAIMS:**

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~striketrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 5-7, 11 and 12 in accordance with the following:

1.       **(Currently Amended)**       A thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region and a plurality of primary crystal grain boundaries, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are not positioned in the LDD or offset region.
2.       **(Original)**       The thin film transistor according to claim 1, wherein a width of an activation layer including the LDD region or offset region is shorter than a distance between the primary crystal grain boundaries.
3.       **(Original)**       The thin film transistor according to claim 1, wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method.
4.       **(Original)**       The thin film transistor according to claim 1, wherein the thin film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent) device.
5.       **(Currently Amended)**       The thin film transistor according to claim 1, wherein the primary crystal grain boundaries are perpendicular to a current direction between ~~active channel regions~~ source and drain regions of the thin film transistor.
6.       **(Currently Amended)**       The thin film transistor according to claim 1, wherein the primary crystal grain boundaries are inclined to a current direction between active ~~channel regions~~ source and drain regions of the thin film transistor at an angle of  $-45^{\circ} \leq \Theta \leq 45^{\circ}$ .

7. **(Currently Amended)** A flat panel display device comprising:  
a thin film transistor comprising:  
an LDD region or offset region, and a plurality of primary crystal grain boundaries,  
wherein the thin film transistor is formed so that the primary crystal grain  
boundaries of a polysilicon substrate are not positioned in the LDD or offset region.
8. **(Original)** The flat panel display device according to claim 7, wherein a width  
of an activation layer including the LDD region or offset region is shorter than a distance  
between the primary crystal grain boundaries.
9. **(Original)** The flat panel display device according to claim 7, wherein the  
polysilicon substrate is formed by a sequential lateral solidification (SLS) method.
10. **(Original)** The flat panel display device according to claim 7, wherein the thin  
film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent)  
device.
11. **(Currently Amended)** The flat panel display device according to claim 7,  
wherein the primary crystal grain boundaries are perpendicular to a current direction between  
~~active channel~~source and drain regions of the thin film transistor.
12. **(Currently Amended)** The flat panel display device according to claim 7,  
wherein the primary crystal grain boundaries are inclined to a current direction between ~~active~~  
~~channel~~source and drain regions of the thin film transistor at an angle of  $-45^\circ \leq \Theta \leq 45^\circ$ .
13. **(Previously Presented)** A thin film transistor (TFT) comprising a lightly  
doped drain (LDD) region or offset region, wherein the thin film transistor is formed so that  
primary crystal grain boundaries of a polysilicon substrate are positioned in channel, source and  
drain regions but not positioned in the LDD or offset region.
14. **(Previously Presented)** A flat panel display device comprising: a thin film  
transistor including an LDD region or offset region, wherein the thin film transistor is formed so

that primary crystal grain boundaries of a polysilicon substrate are positioned in a channel, source and drain regions but not positioned in the LDD or offset region.